Fig. 1 PRIOR ART

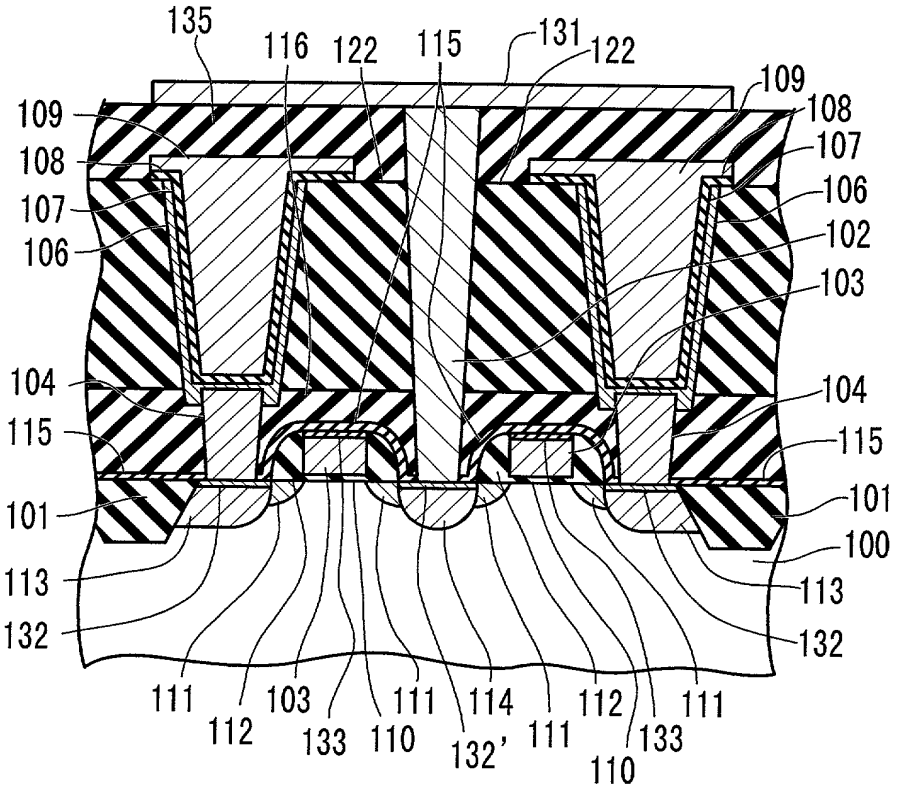


Fig. 2

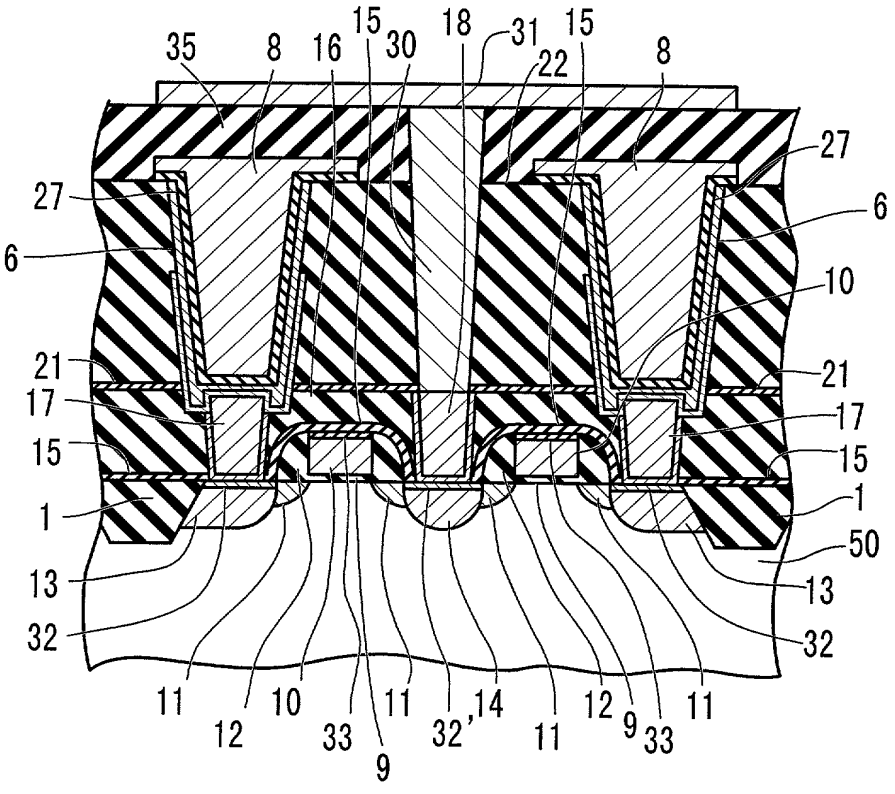

35
8
16
15
30
18
31
22
15
8
27
27
6
6
10
21
21
17
17
15
15
1
1
50
13
13
32
32
11
12
10
33
11
9
32'
14
11
12
9
33
11

Fig. 3

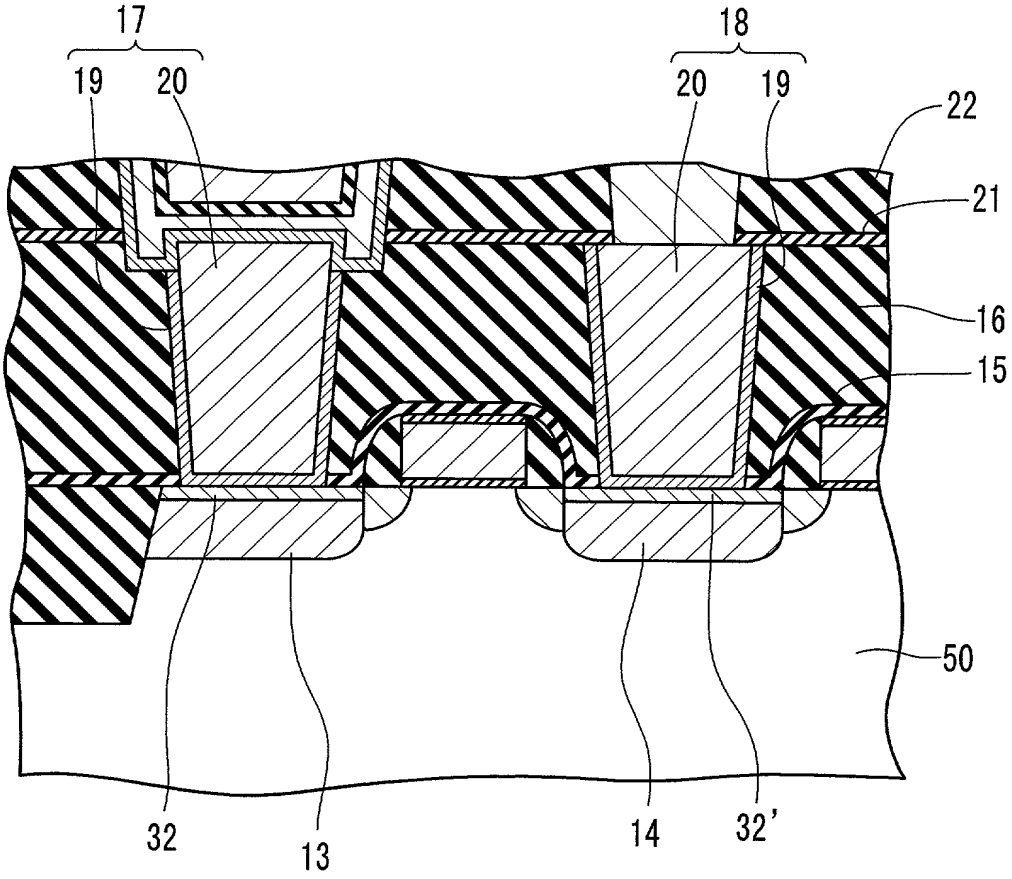


Fig. 4

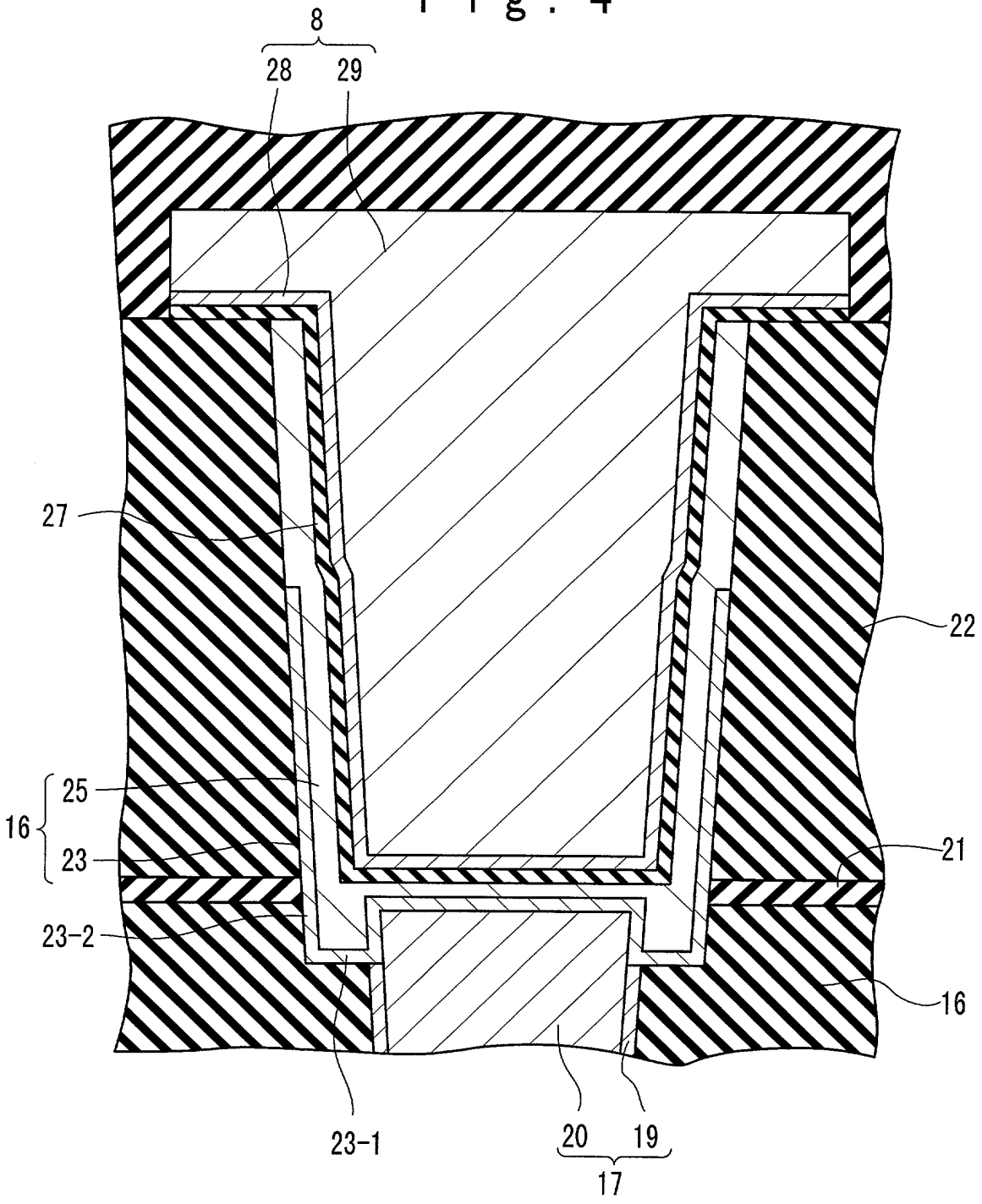


Fig. 5

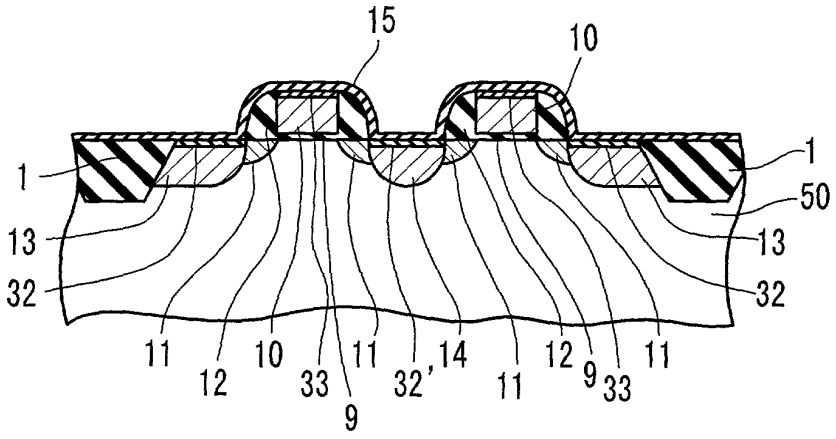


Fig. 6

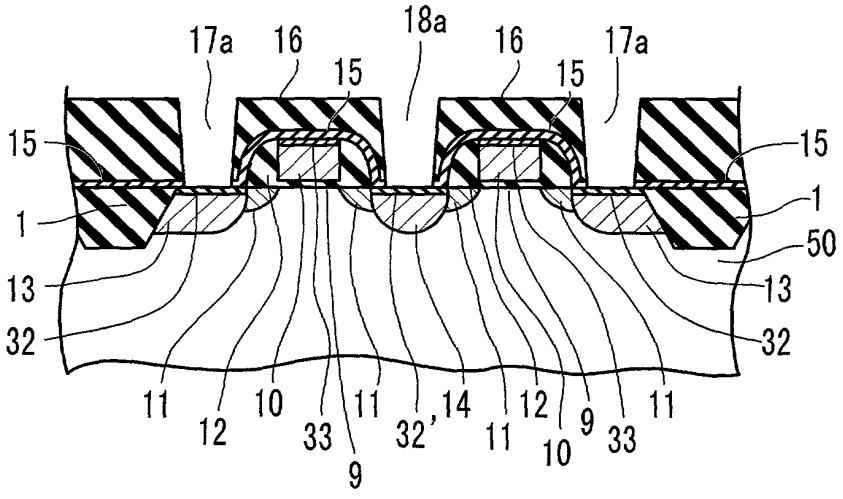

17a
16
18a
16
17a
15
15
15
15
1
1
50
13
13
32
32
11
12
10
33
11
9
32'
14
11
12
10
9
33
11

Fig. 7

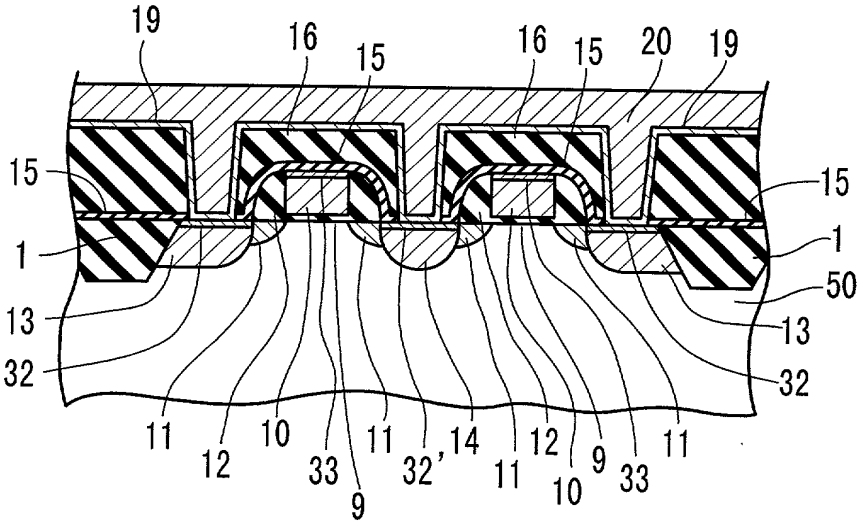

19
16
15
16
15
20
19
15
15
1
1
50
13
13
32
32
11
12
10
33
9
11
32'
14
11
12
10
9
33
11

Fig. 8

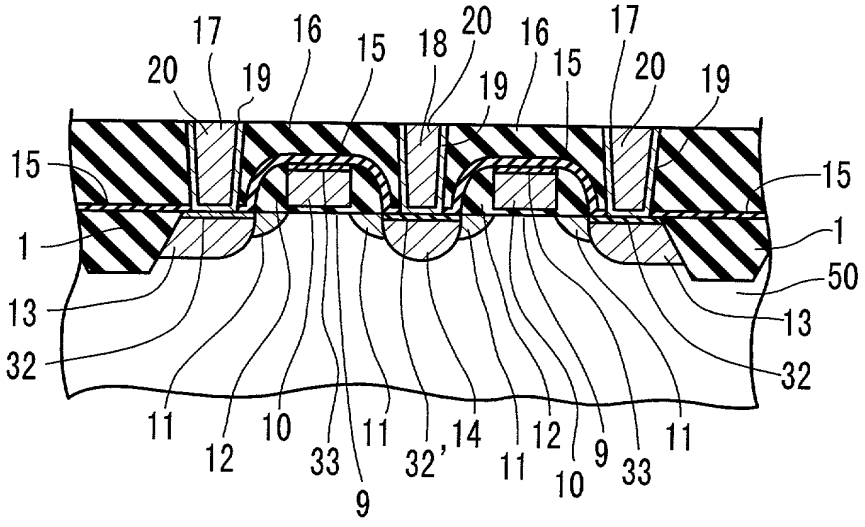

17
16
15
18
20
16
17
20
19
20
19
19
15
15
1
1
50
13
13
32
32
11
12
10
33
11
9
32'
14
11
12
10
9
33
11

Fig. 9

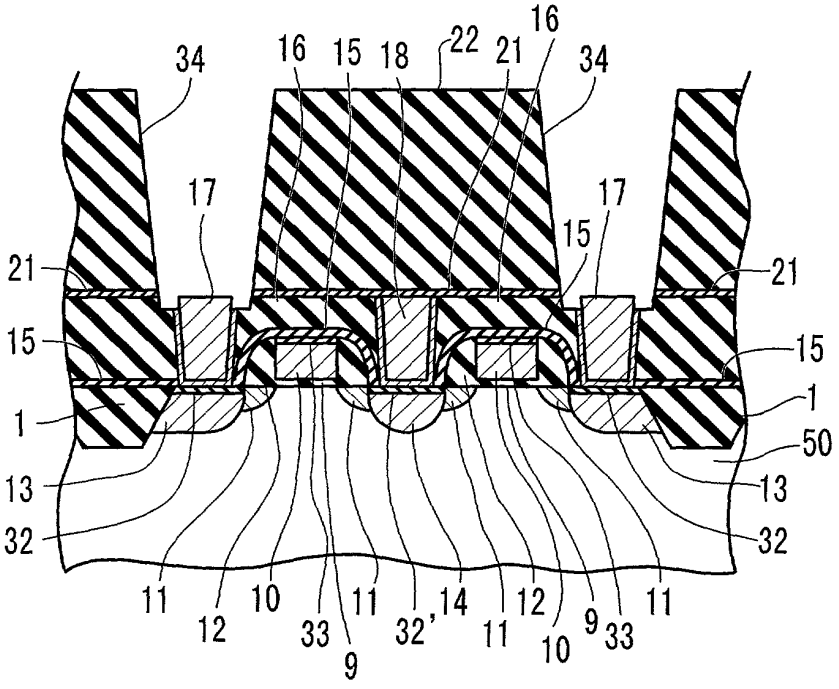


Fig. 10

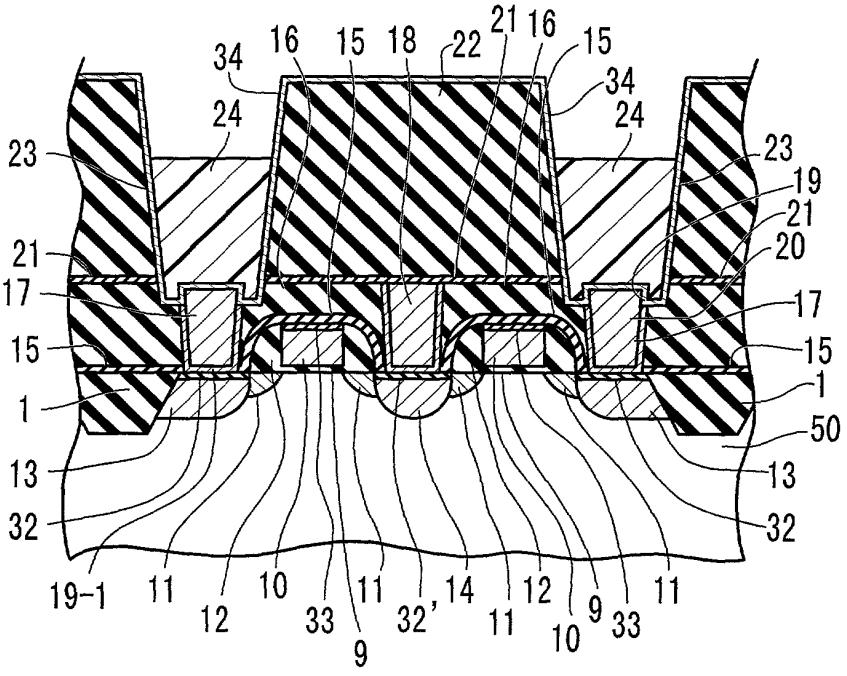

34
16
15
18
22
21
16
15
34
24
24
23
23
19
21
21
20
17
17
15
15
1
1
50
13
13
32
32
19-1
11
12
10
33
9
11
32'
14
11
12
10
9
33
11

Fig. 11

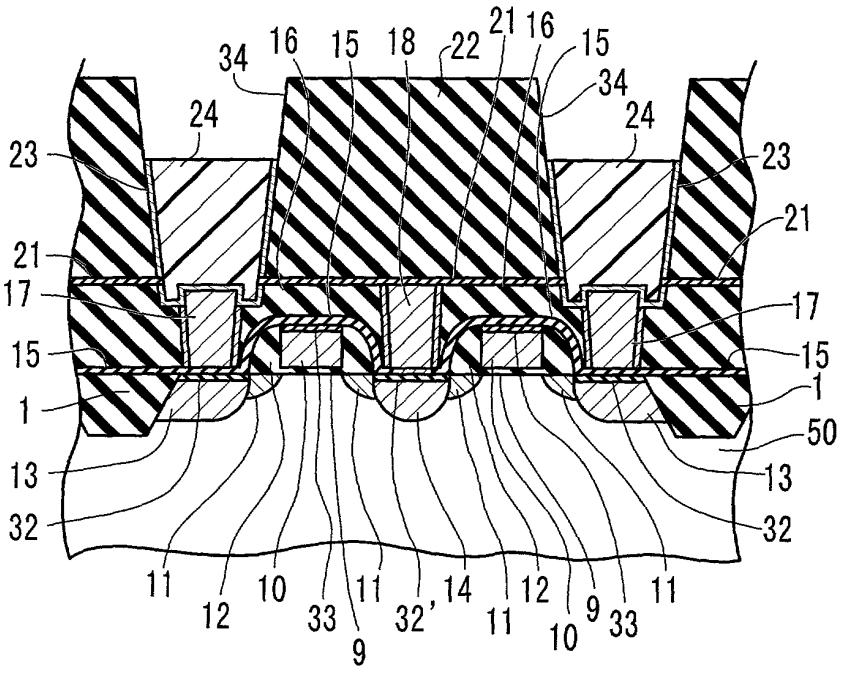

34
16
15
18
22
21
16
15
34
24
24
23
23
21
21
17
17
15
15
1
1
50
13
13
32
32
11
12
10
33
11
9
32'
14
11
12
10
9
33
11

Fig. 12

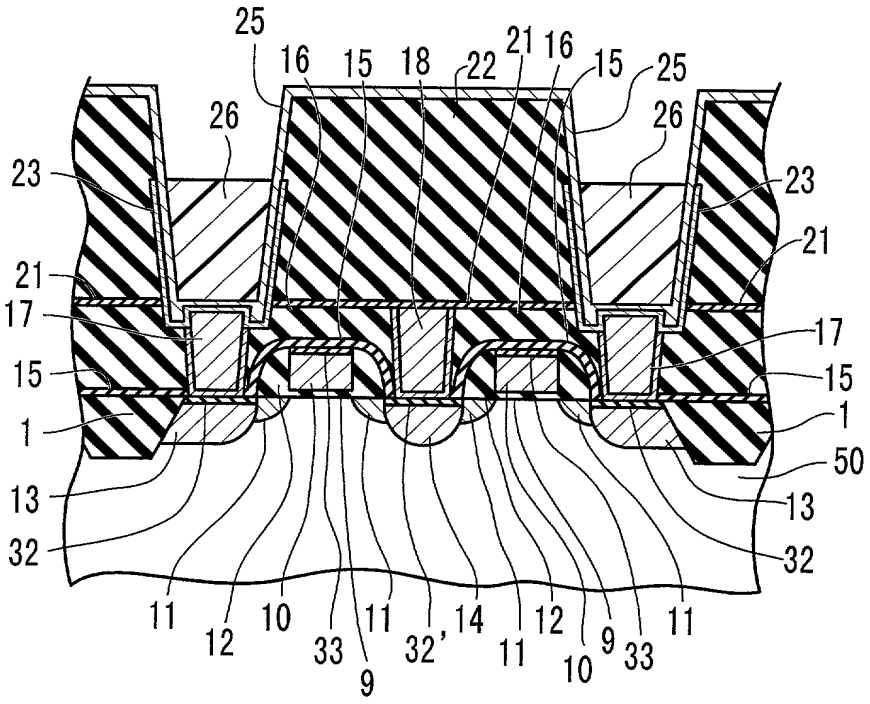

25
16
15
18
22
21
16
15
25
26
26
23
23
21
21
17
17
15
15
1
1
50
13
13
32
32
11
12
10
33
11
9
32'
14
11
12
10
9
33
11

Fig. 13

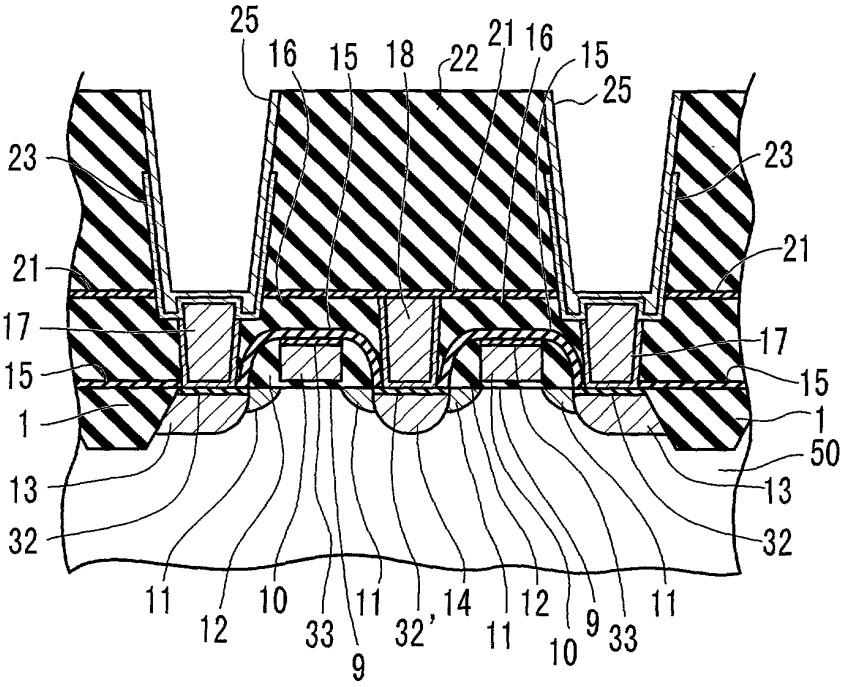

25
16
15
18
22
21
16
15
25
23
23
21
21
17
17
15
15
1
1
50
13
13
32
32
11
12
10
33
11
9
32'
14
11
12
10
9
33
11

Fig. 14

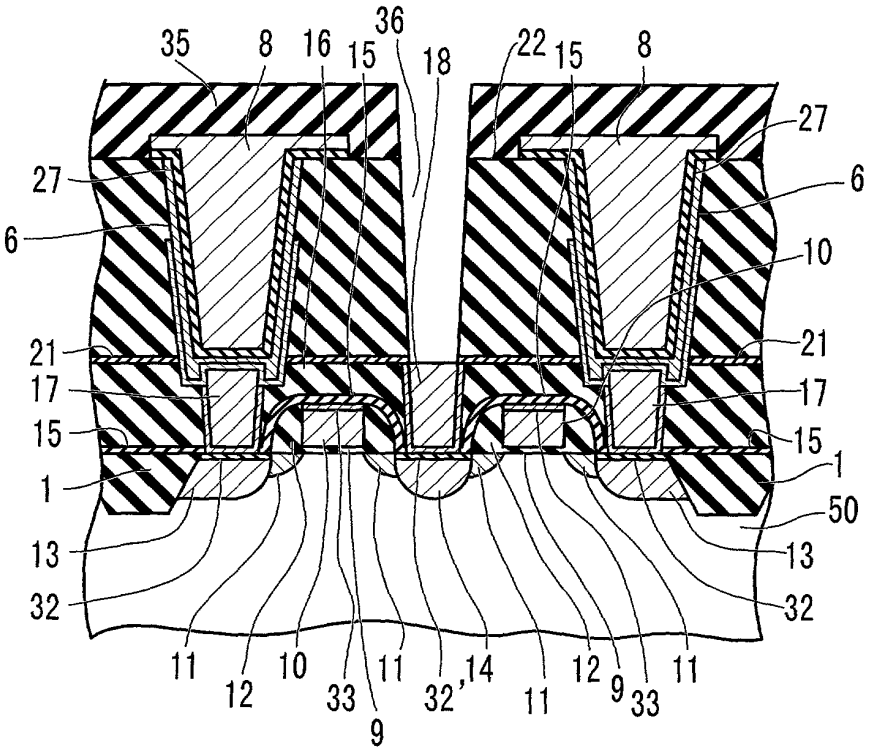

35
8
16
15
36
18
22
15
8
27
27
6
6
10
21
21
17
17
15
15
1
1
50
13
13
32
32
11
12
10
33
11
9
32'
14
11
12
9
33
11

Fig. 15

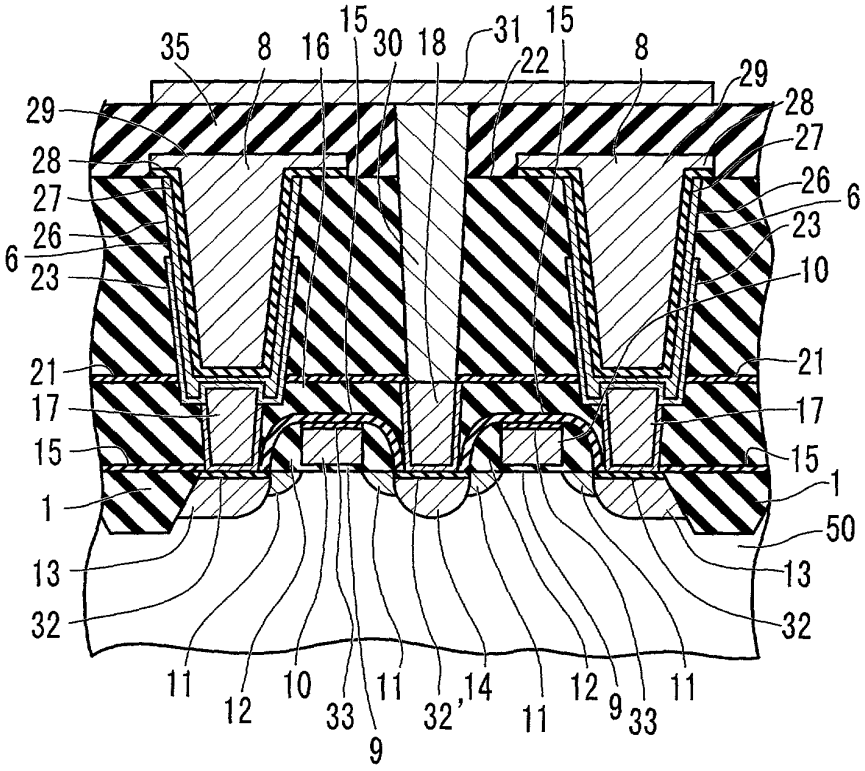

35
8
16
15
30
18
31
22
15
8
29
28
27
26
6
23
10
21
17
15
1
50
13
32
11
12
10
33
9
11
32
14
11
12
9
33
11

Fig. 16

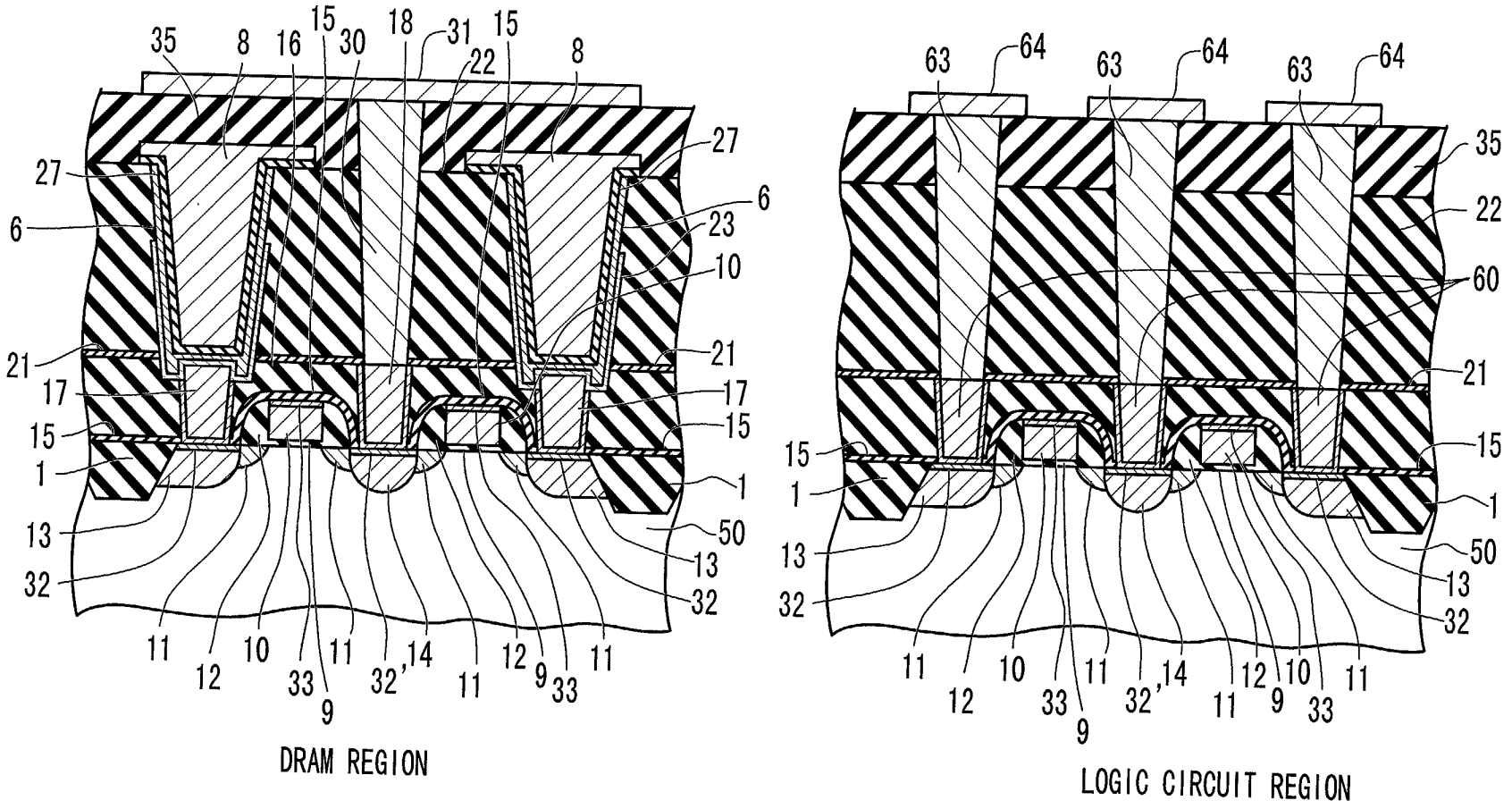
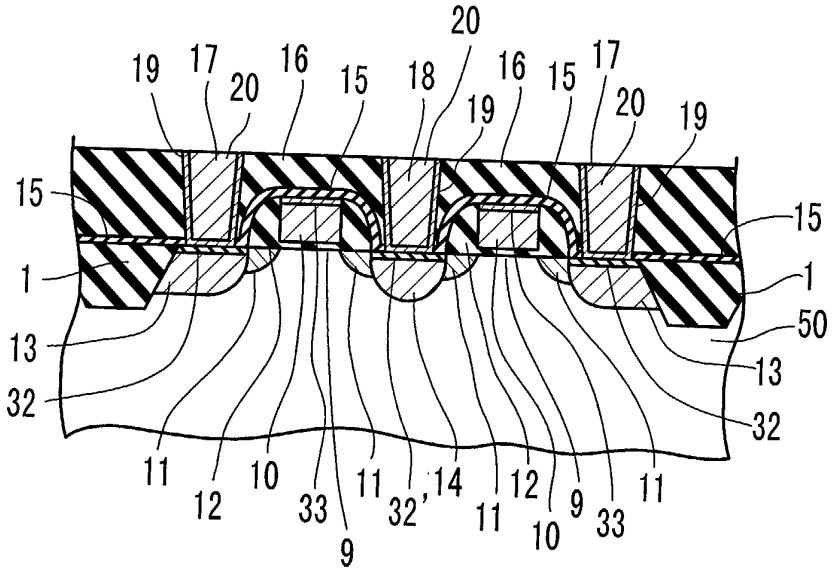
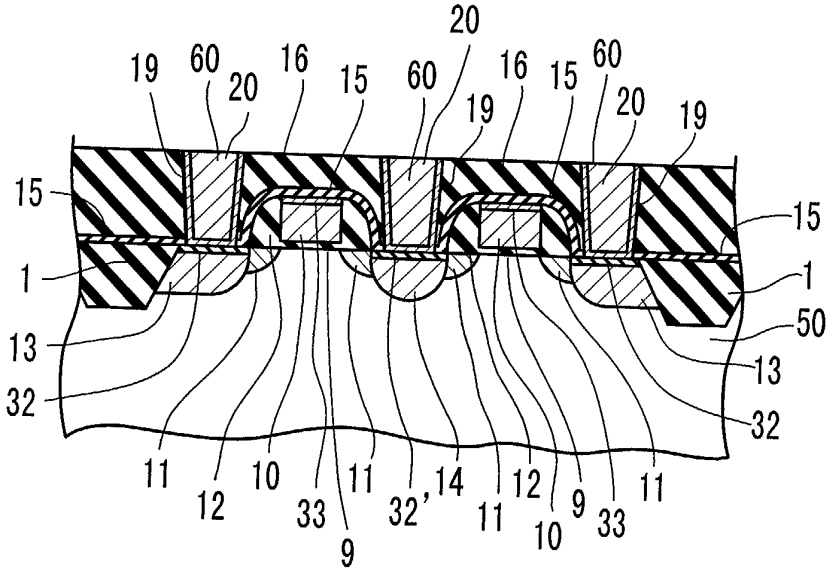

35
8
16
15
30
18
31
22
15
8
27
27
6
6
23
10
21
21
17
17
15
15
1
1
13
50
13
32
32
11
12
10
33
9
11
32'
14
11
12
9
33
11
63
64
63
64
63
64
35
22
60
21
15
15
1
1
13
50
13
32
32
11
12
10
33
9
11
32'
14
11
12
9
10
33
11
DRAM REGION
LOGIC CIRCUIT REGION

Fig. 17

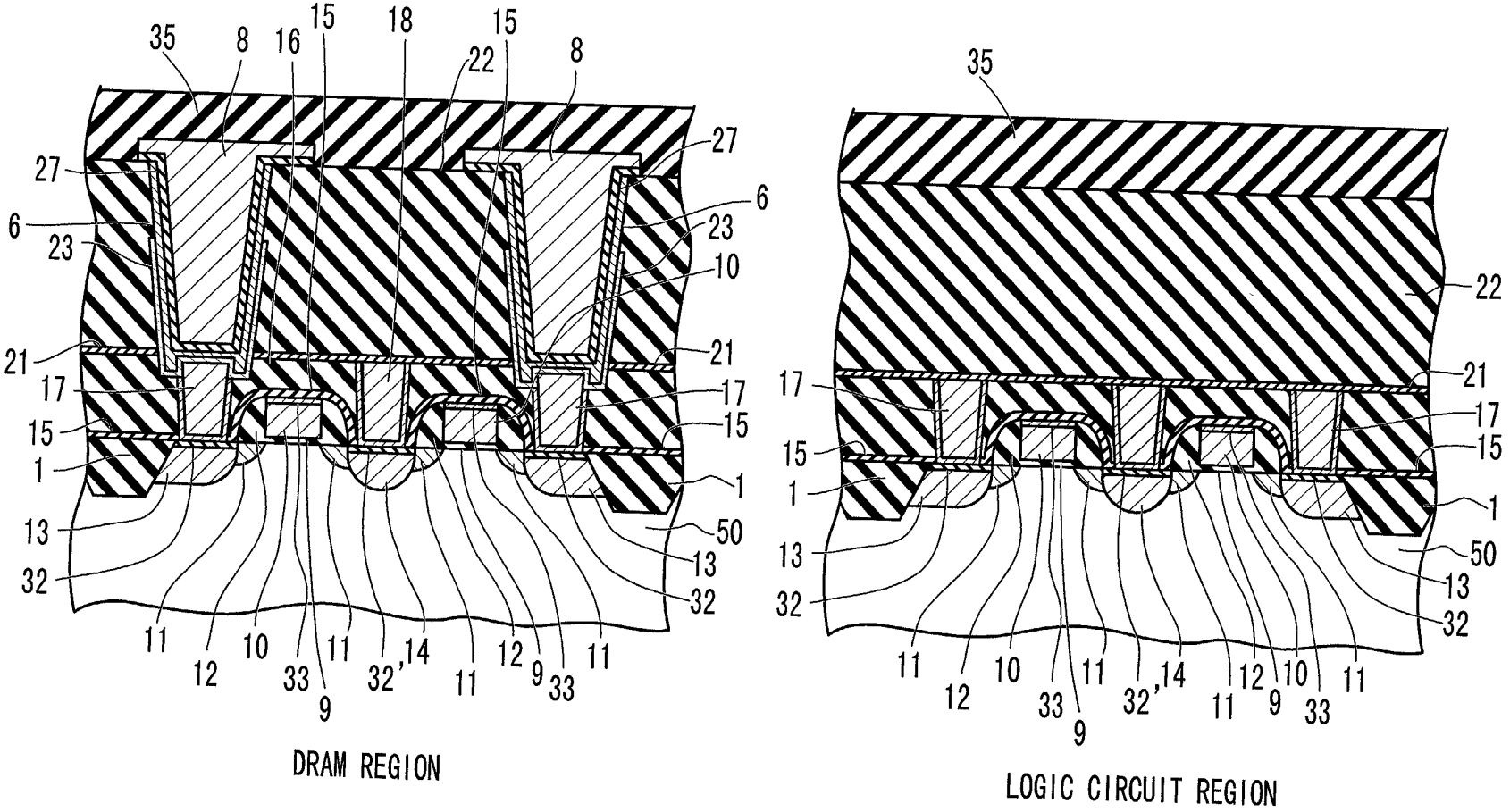


DRAM REGION



LOGIC CIRCUIT REGION

Fig. 18



DRAM REGION

LOGIC CIRCUIT REGION

Fig. 19

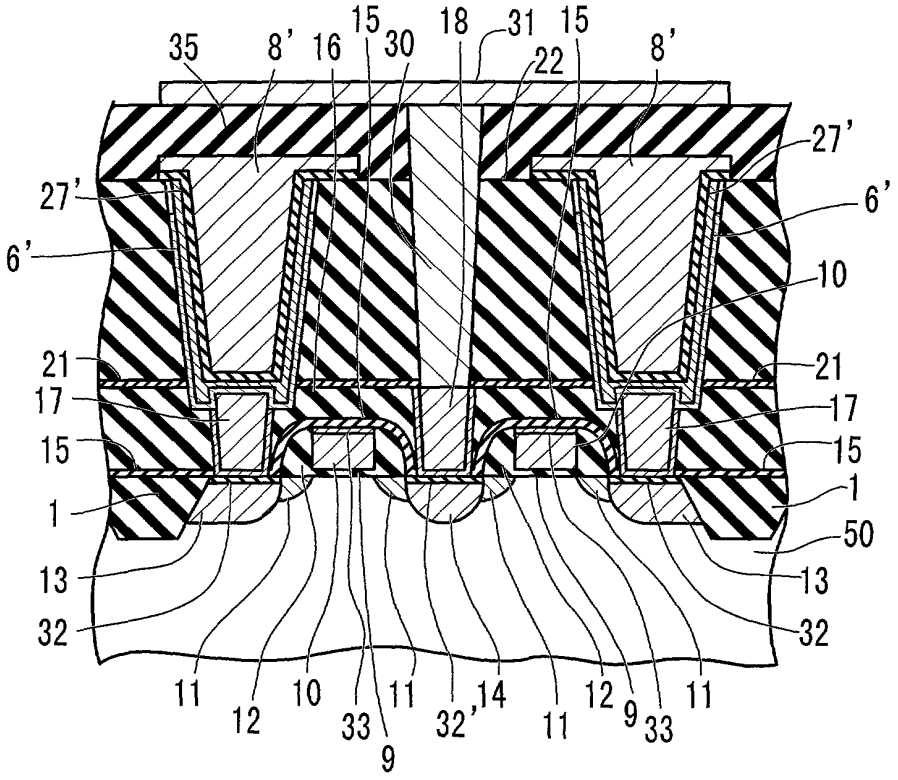

35
8'
16
15
30
18
31
15
22
8'
27'
27'
6'
6'
10
21
21
17
17
15
15
1
1
50
13
13
32
32
11
12
10
33
11
9
32'
14
11
12
9
33
11

Fig. 20

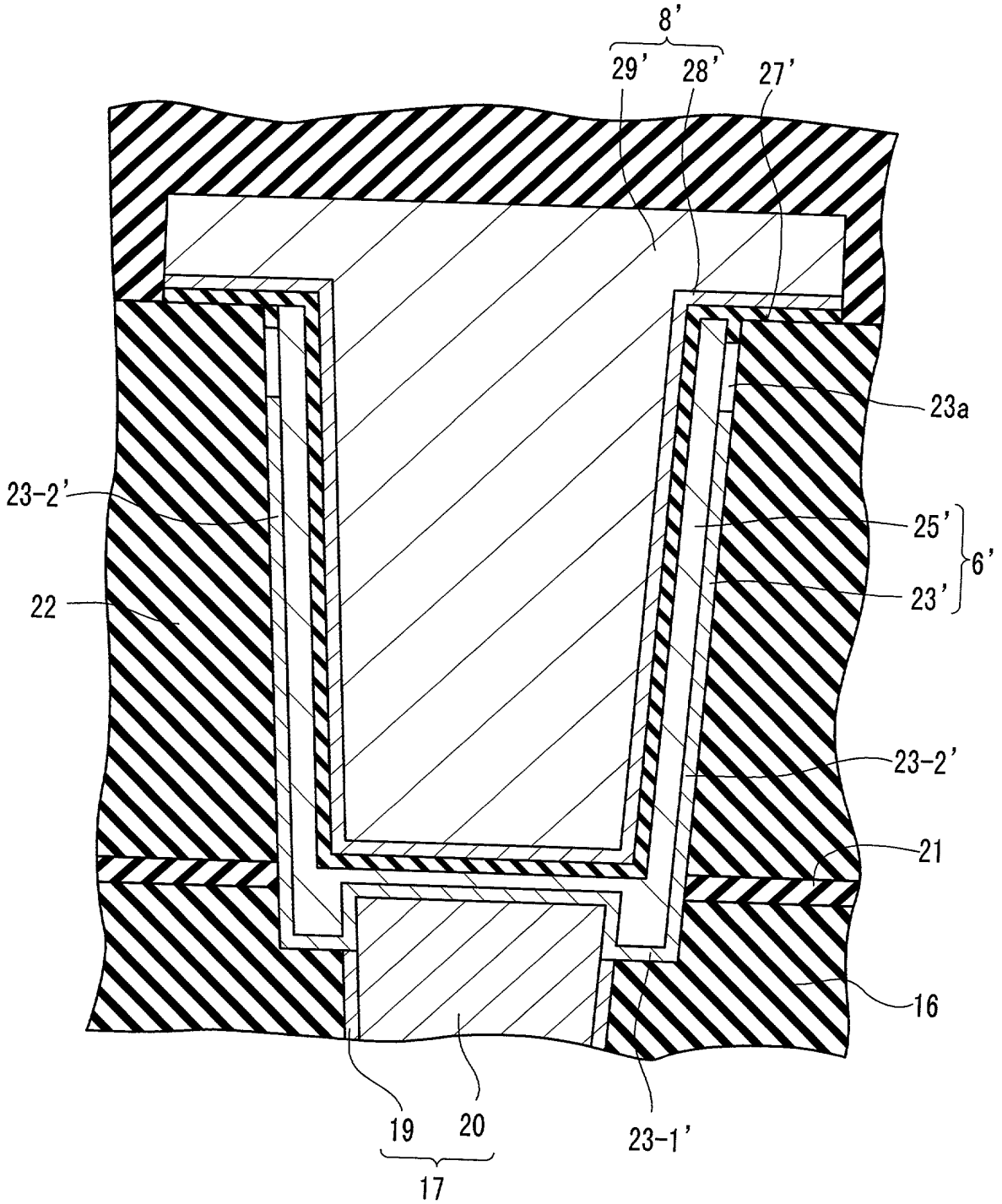


Fig. 21

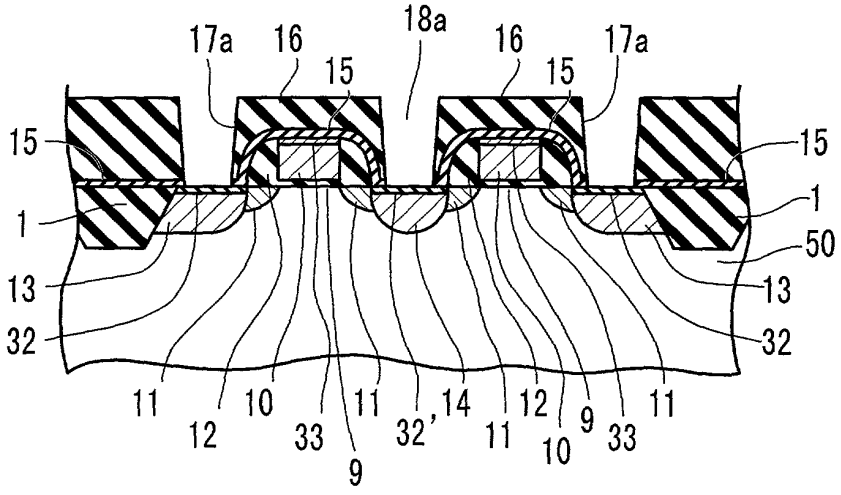

17a
16
18a
16
17a
15
15
15
15
1
1
50
13
13
32
32
11
12
10
33
11
9
32'
14
11
12
10
9
33
11

Fig. 22

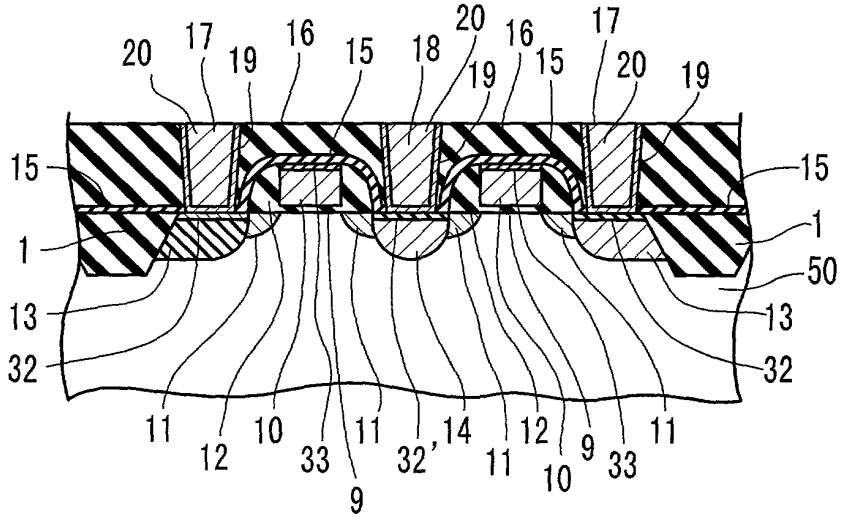

20
17
19
16
15
18
20
19
16
15
17
20
19
15
15
1
1
50
13
13
32
32
11
12
10
33
11
9
32'
14
11
12
10
9
33
11

Fig. 23

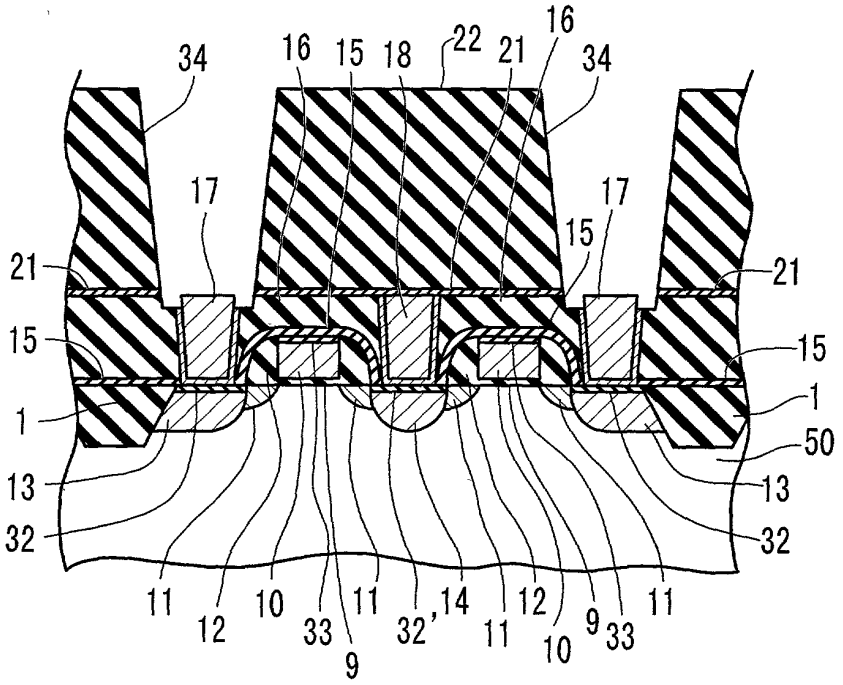

34
16
15
18
22
21
16
34
17
17
15
21
21
15
15
1
1
50
13
13
32
32
11
12
10
33
11
9
32'
14
11
12
10
9
33
11

Fig. 24

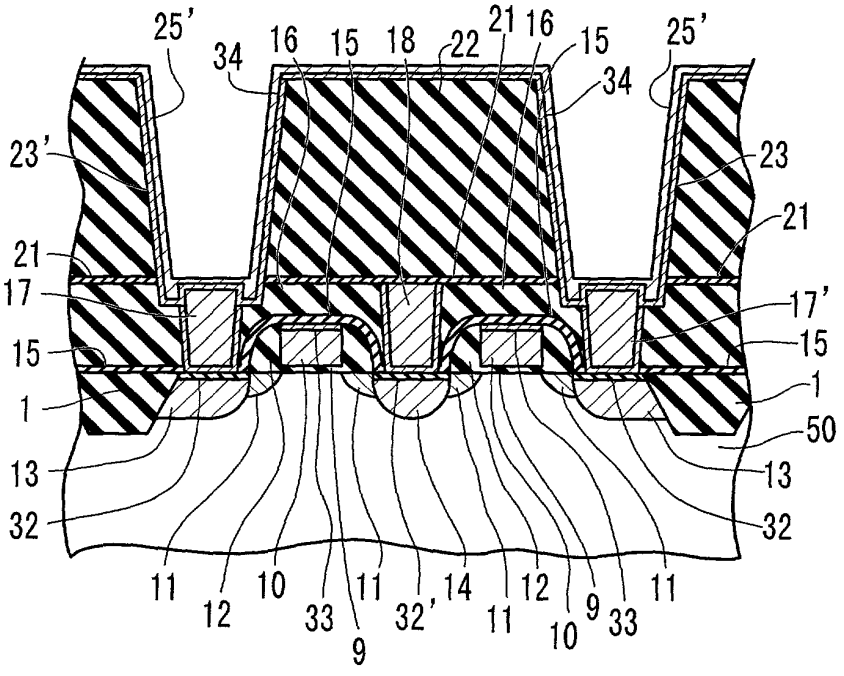

25'
34
16
15
18
22
21
16
15
25'
34
23'
23
21
21
17
17'
15
15
1
1
50
13
13
32
32
11
12
10
33
11
9
32'
14
11
12
10
9
33
11

Fig. 25

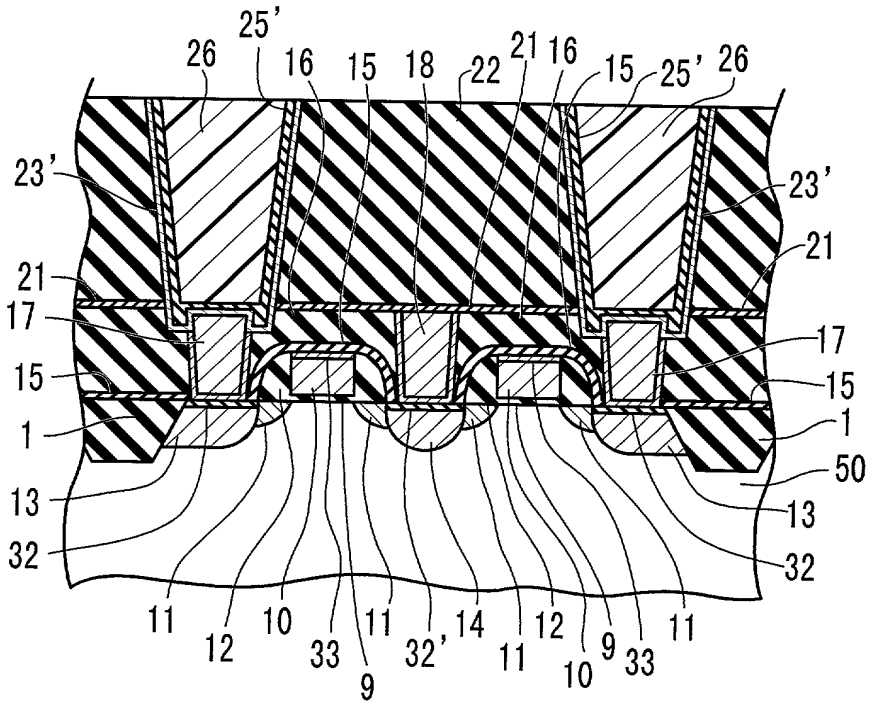

25'
26
16
15
18
22
21
16
15
25'
26
23'
23'
21
21
17
17
15
15
1
1
50
13
13
32
32
11
12
10
33
11
9
32'
14
11
12
10
9
33
11

Fig. 26

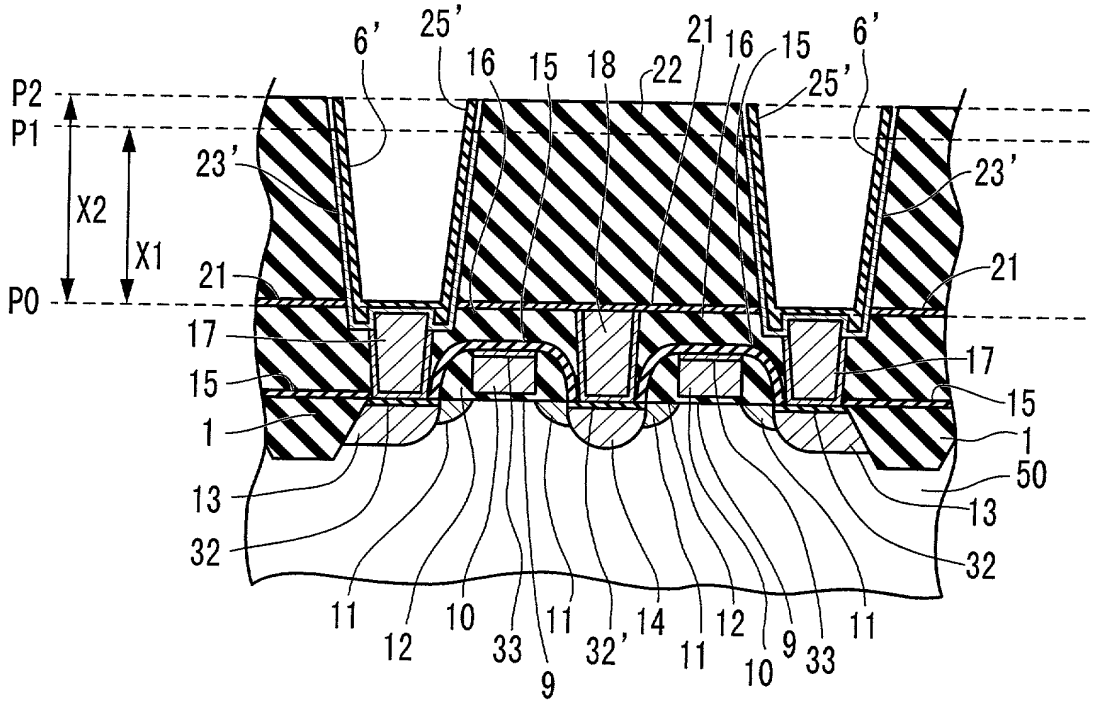

6'
25'
16
15
18
22
21
16
15
6'
25'
P2
P1
P0
X2
X1
23'
23'
21
21
17
17
15
15
1
1
50
13
13
32
32
11
12
10
33
11
9
32'
14
11
12
10
9
33
11

Fig. 27

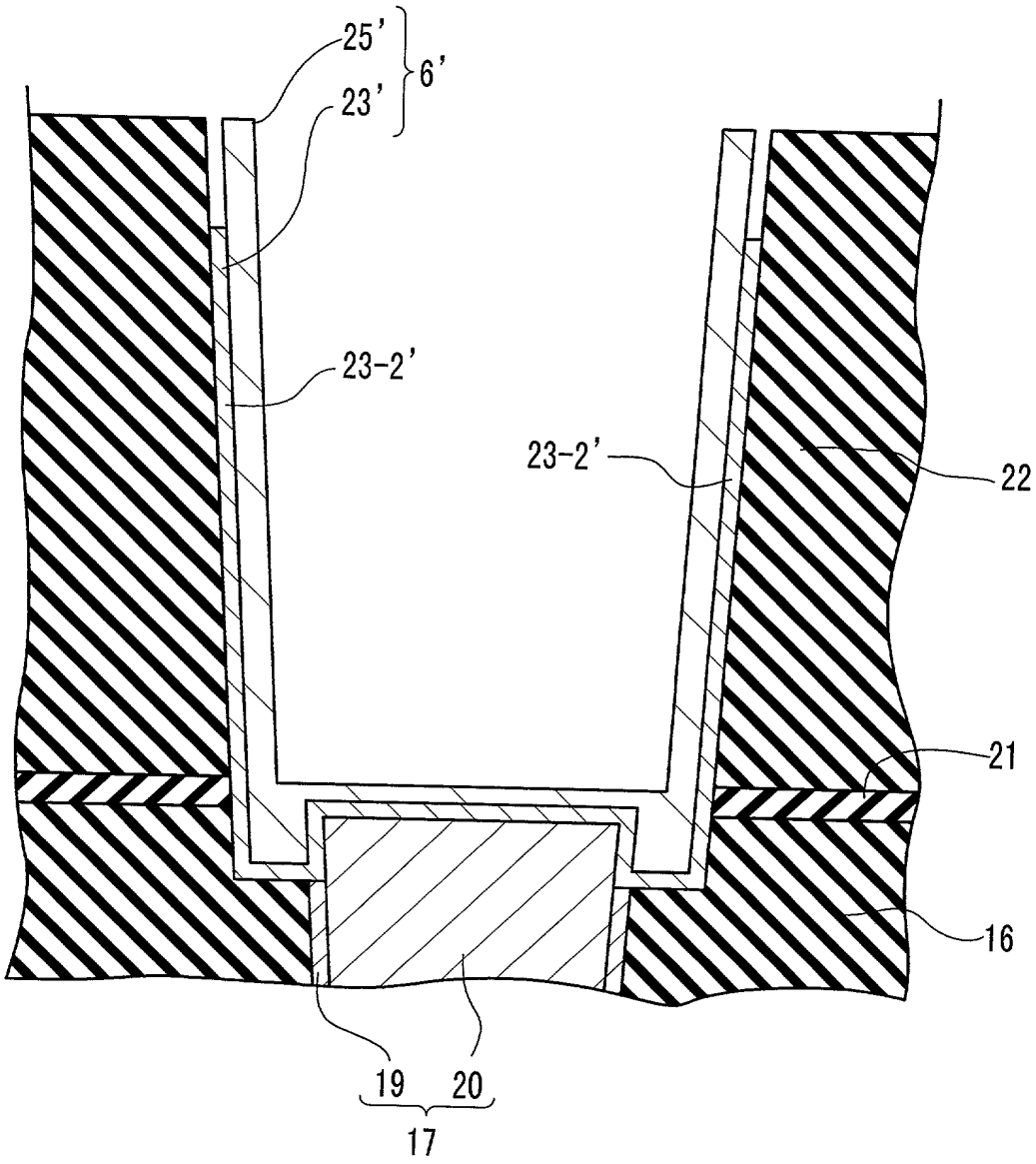


Fig. 28

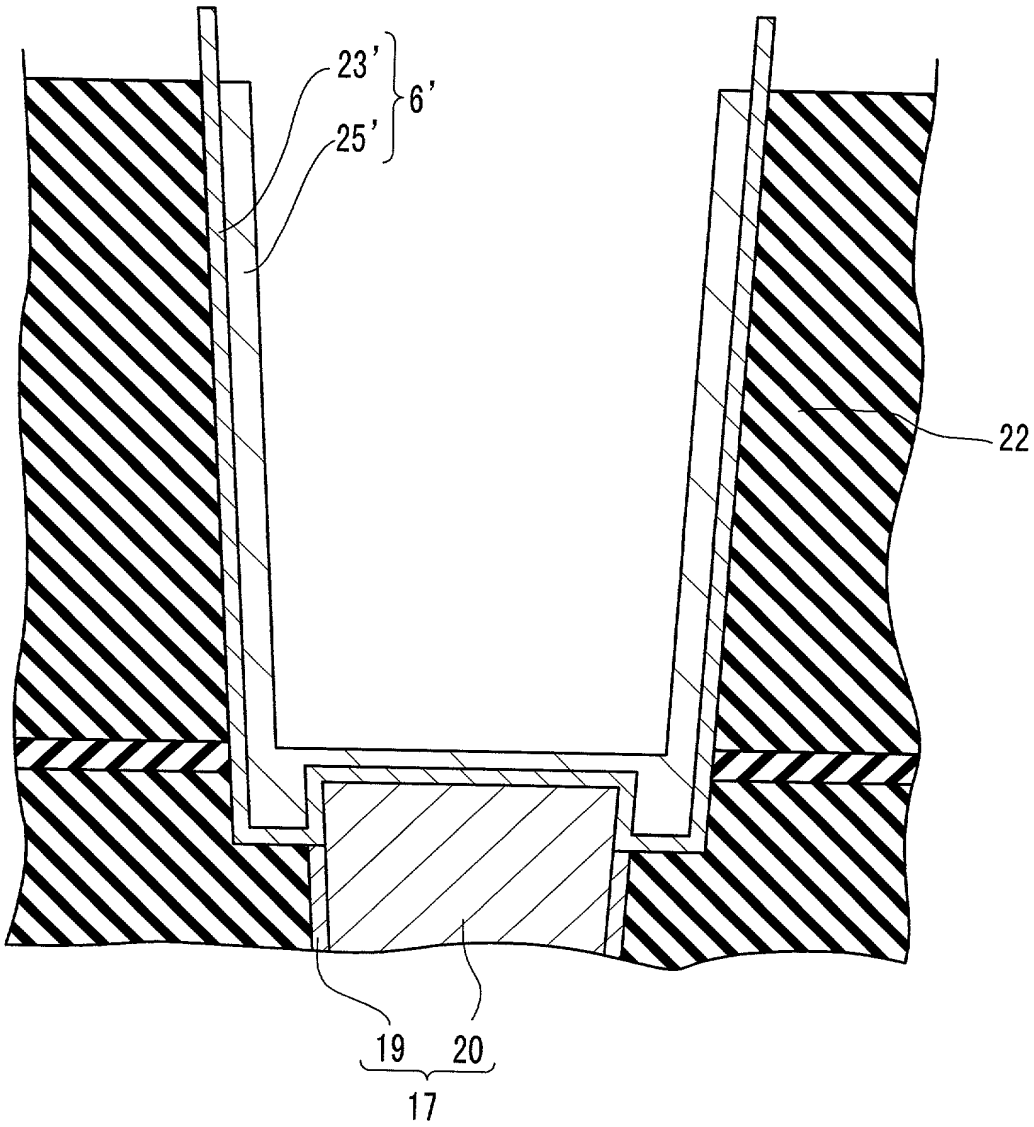


Fig. 29

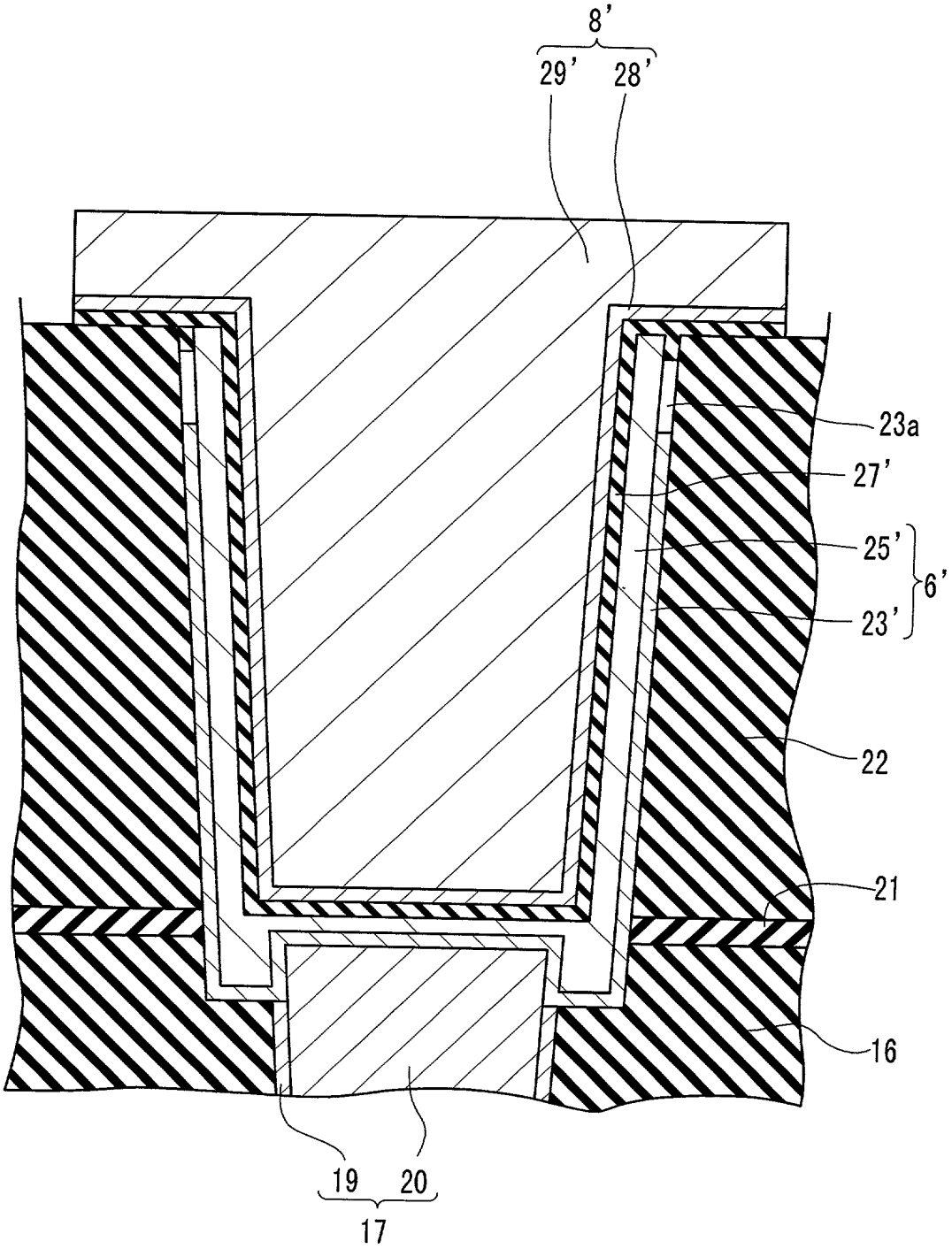


Fig. 30

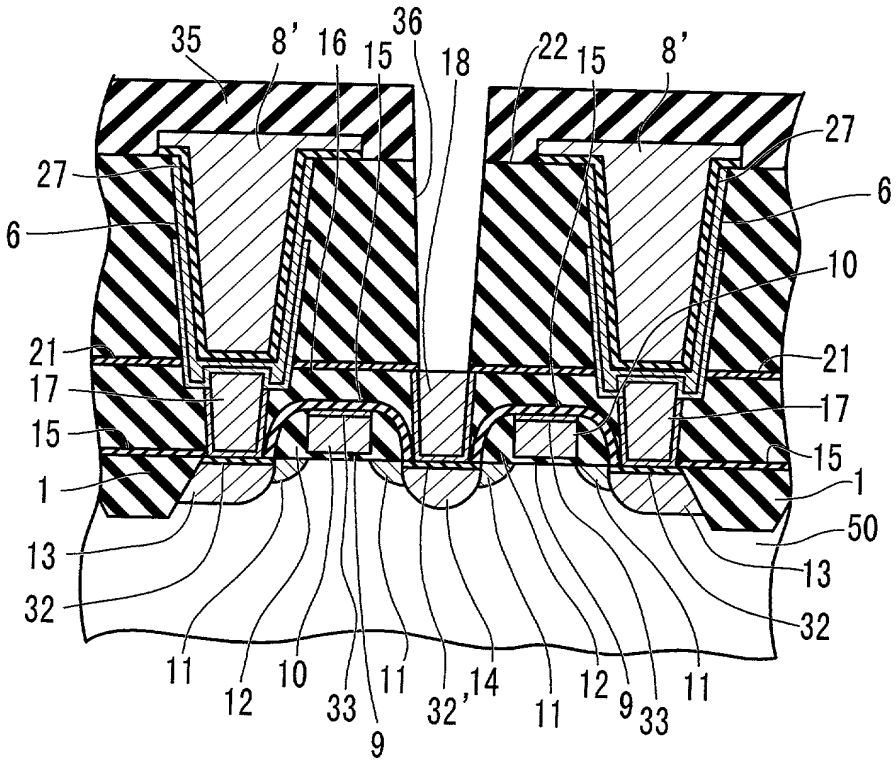
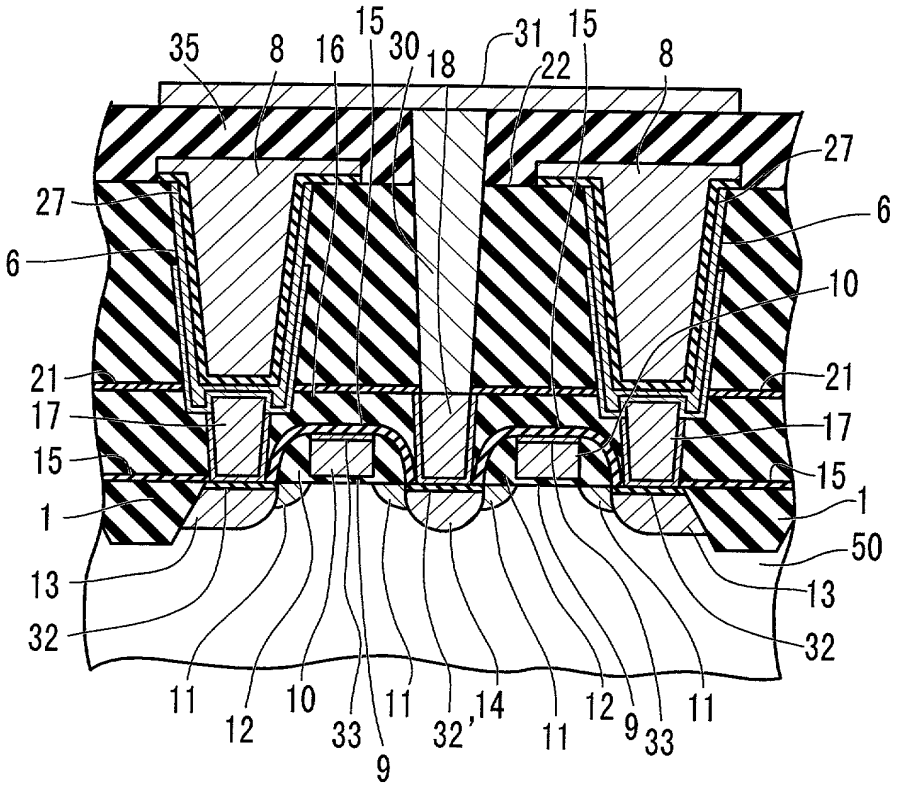

35
8'
16
15
36
18
22
15
8'
27
27
6
6
10
21
21
17
17
15
15
1
1
50
13
13
32
32
11
12
10
33
11
9
32'
14
11
12
9
33
11

Fig. 31


35
8
16
15
30
18
31
22
15
8
27
27
6
6
10
21
21
17
17
15
15
1
1
50
13
13
32
32
11
12
10
33
9
11
32'
14
11
12
9
33
11